

Fig. 1

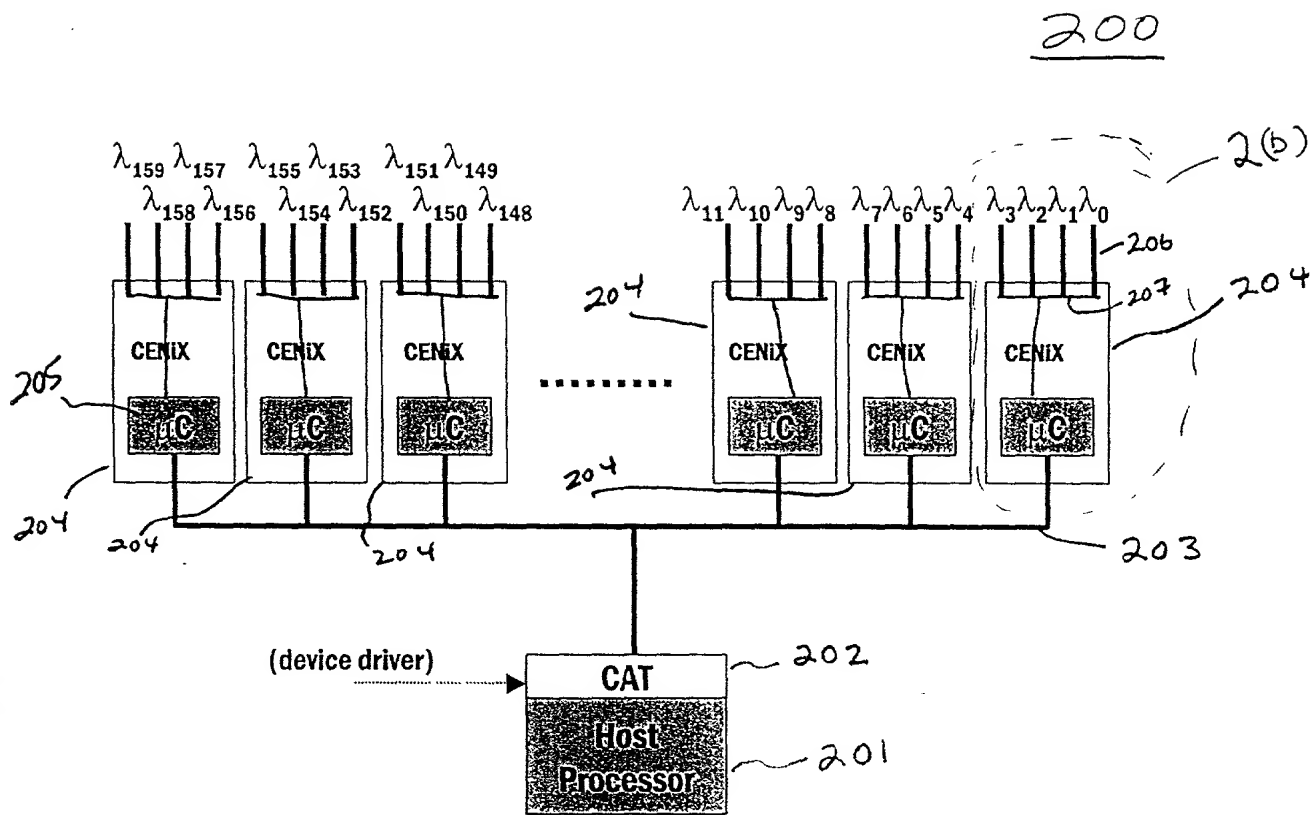


Fig. 2 (a)

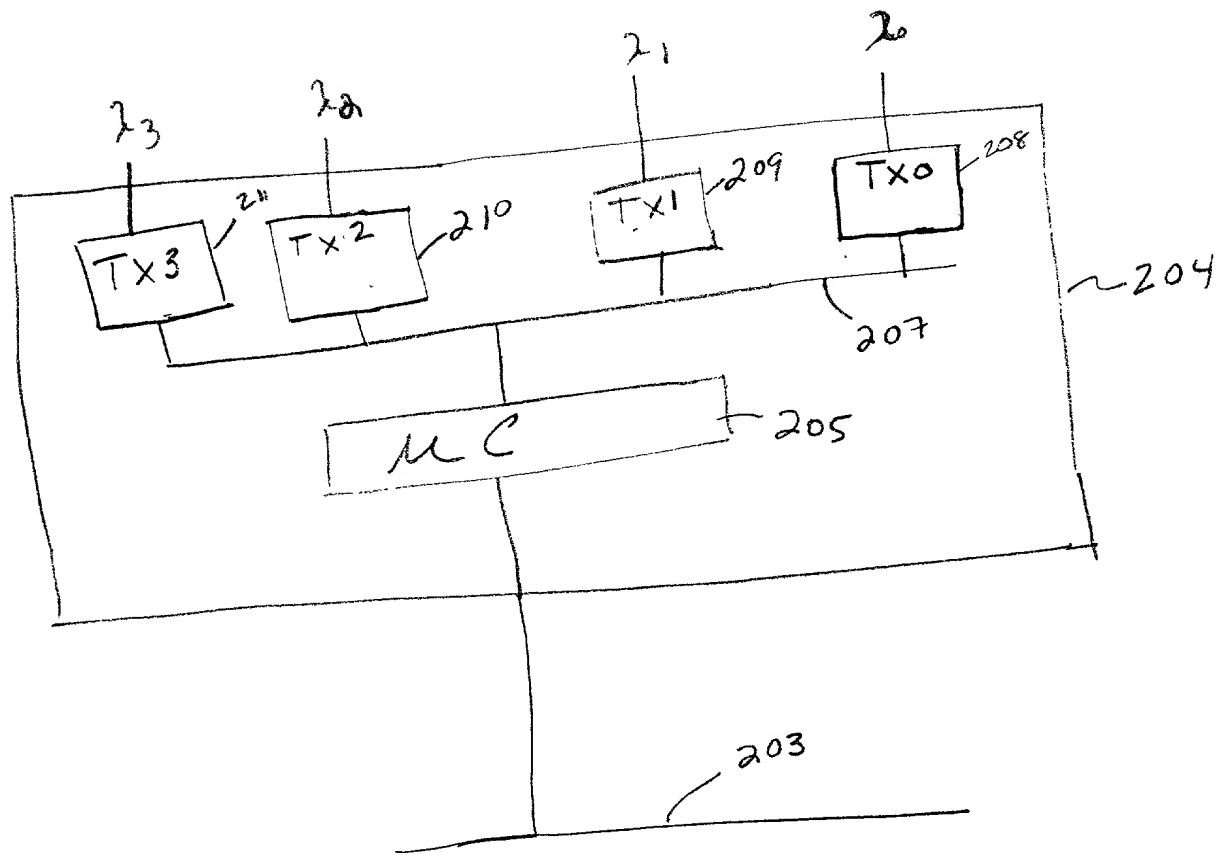


Fig. 2(b)

(Channel Access Table Example)

212

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	0	0x200
2	0	0x400
3	0	0x600
4	4	0x000
5	4	0x200
6	4	0x400
7	4	0x600
⋮	⋮	⋮
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

Fig. 2(c)

Fig. 3

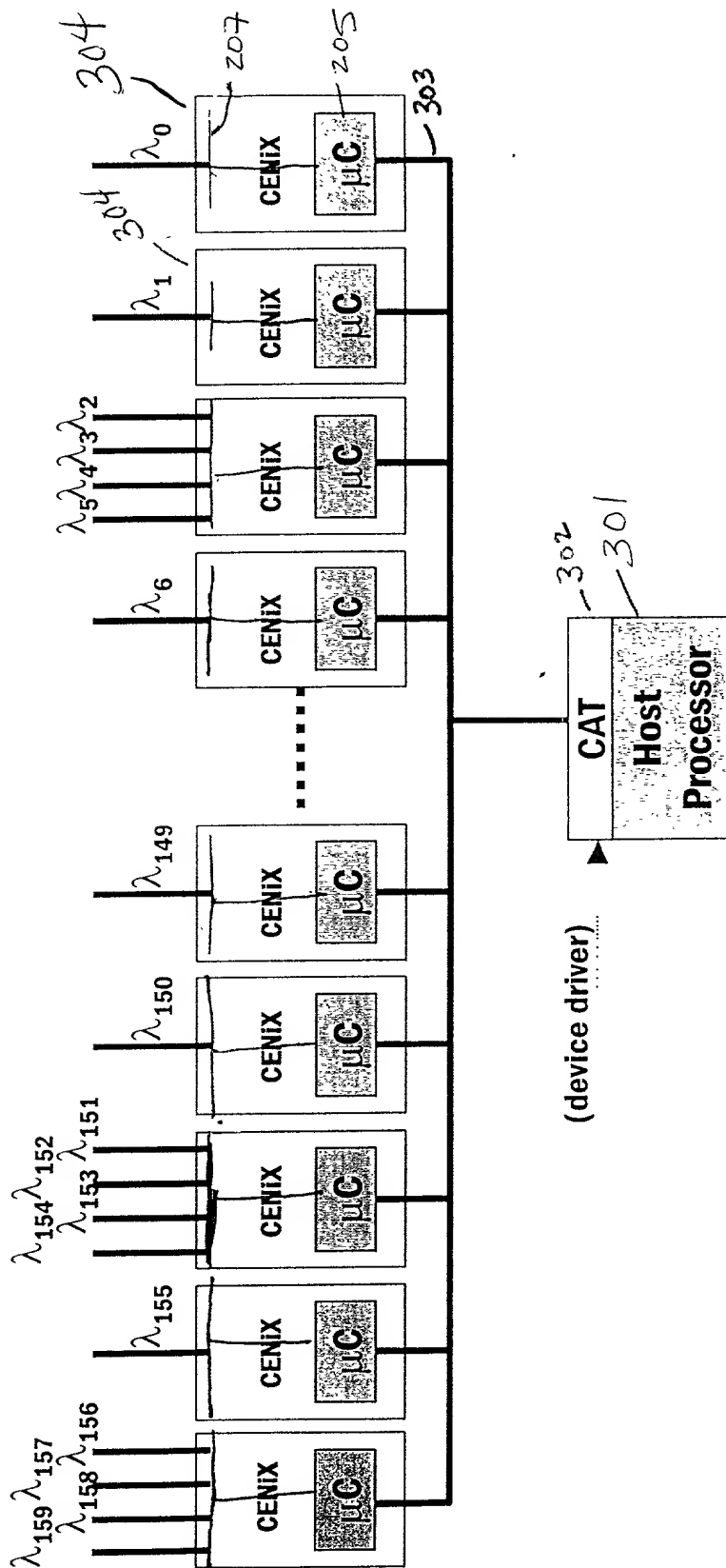


Fig. 4

400

(Channel Access Table Example)

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	1	0x000
2	2	0x000
3	2	0x200
4	2	0x400
5	2	0x600
6	6	0x000
⋮	⋮	⋮
154	151	0x600
155	155	0x000
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

Fig. 5

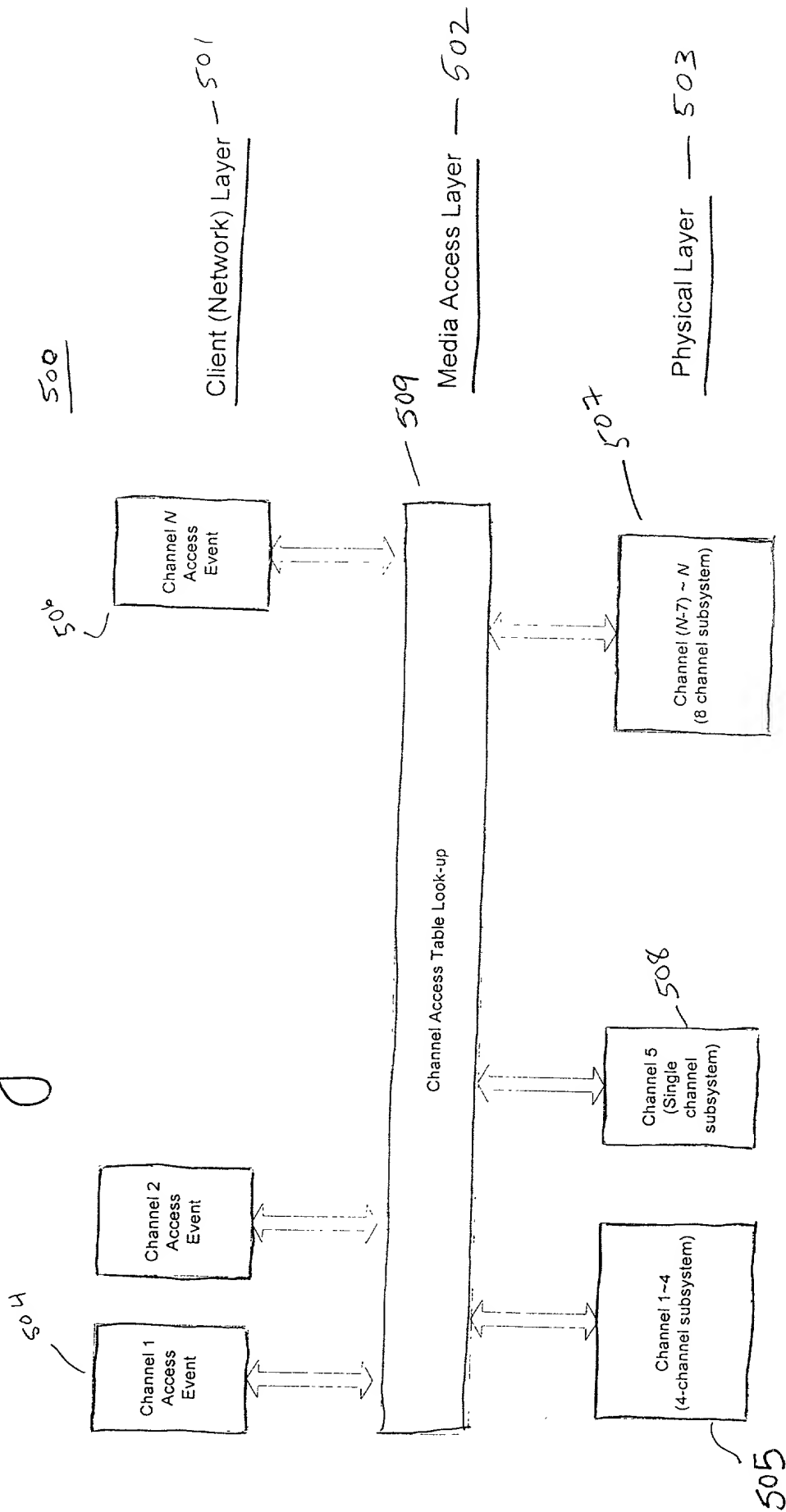
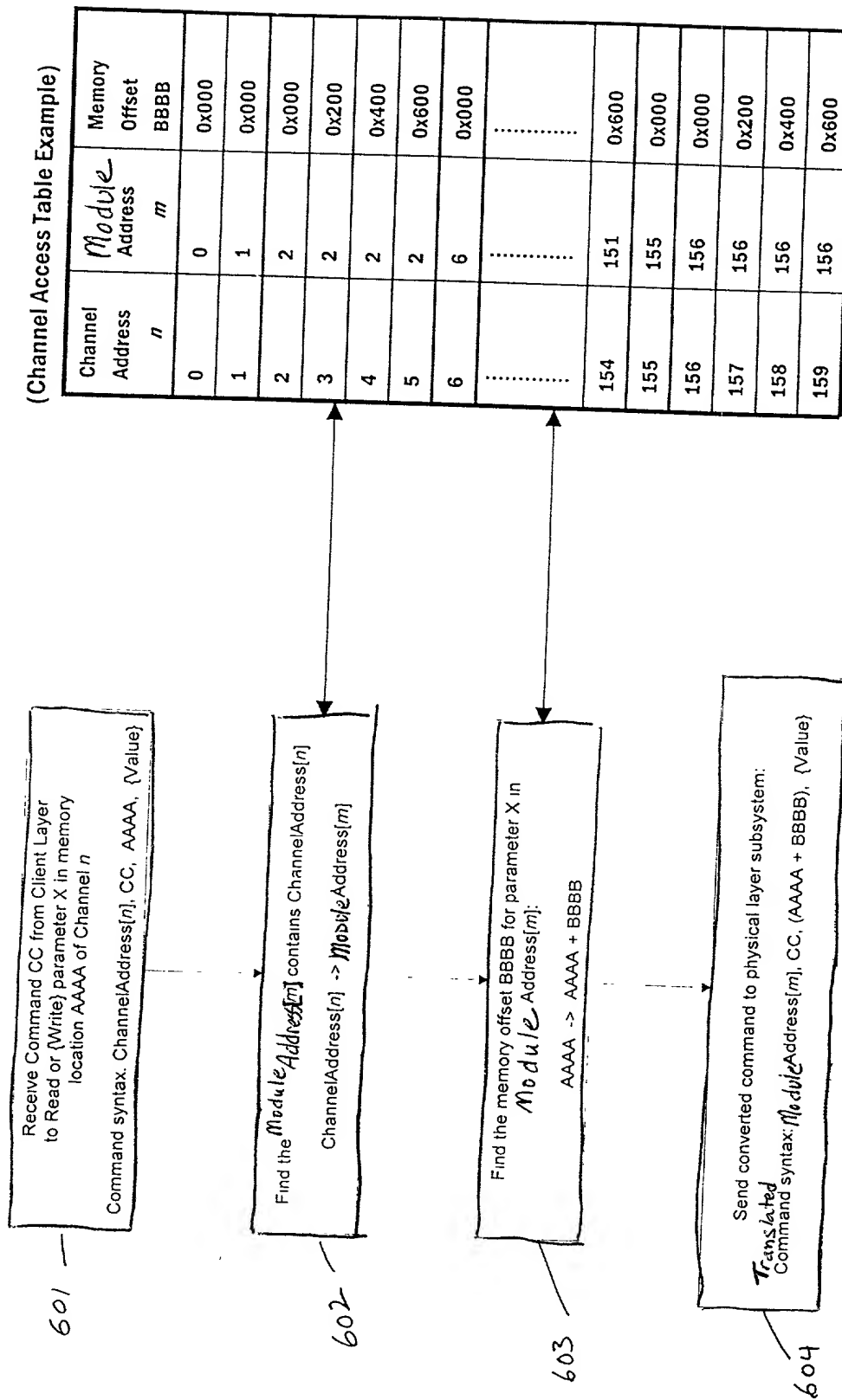


FIG. 6



Channel 1 Memory Map

0x0000	Tx Temp
0x0002	Tx Bias
0x0004	Rx Power
.....

701

Channel 2 Memory Map

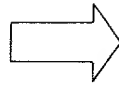
0x0000	Tx Temp
0x0002	Tx Bias
0x0004	Rx Power
.....

702

Channel 3 Memory Map

0x0000	Tx Temp
0x0002	Tx Bias
0x0004	Rx Power
.....

703



CAT Memory Offset = 0x0000

CAT Memory Offset = 0x0100

CAT Memory Offset = 0x0200

0x0000	Channel 1
0x0002	Memory Map
.....
0x0100	Channel 2
0x0102	Memory Map
.....
0x0200	Channel 3
0x0202	Memory Map
.....

Fig. 7